Fine Control Over Ultra-Low Voltage Current Using Fermionic Loops

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Introduction

The limits of transistor ephemerality are dictated not only by the rate of electron dissipation of semiconductor materials, but also by level of voltage supplied to those transistors. The more voltage used, the longer a period of inactivity is required for a transistor's charge to dissipate.

With the prospect of fermionic processors now close at hand, tolerances for transistor ephemerality will undoubtedly become more exacting in systems employing light-speed electrons.

The use of ultra-low voltages in processor architectures presents two primarily problems: The possibility of either an over-abundance or paucity of electrons being supplied to the processor. In the case of over-abundance, a processor will destabilize due to the failure of one or more transistors to fully discharge in the allotted time. In the case of a paucity of electrons, the processor will destabilize as a result of intended signals failing to reach their destination.

In a fermionic processor, data pipelines have a fixed maximal capacity for superconduction based upon the product of the strength of the neutrino vacuum and the intensity of the Spin-Alterative Photon Source (SAPS.) Although these pipelines could convey electrons at 100% of light speed, the electrons would be reduced in speed during their time flowing through transistors. Conventional transistors would cause electrons to "bunch up" in such a computing architecture and would cause current that had been well-regulated when it began its journey to quickly become unsuitable for the application.

In order for a fermionic processor to function reliably utilizing non-superconducting components sc. the transistors themselves, the voltage must be re-regulated each time it exits from a transistor.

Abstract

The same mechanism described on 30 November 2023 for conferring a superconductive capacity to a specialized data pipeline composed largely of conventional materials may be used additionally as a voltage regulator for ultra-low voltages through a process that may be termed Electron-Fermion Sifting (EFS.)

In such a proposed processor, it would be necessary for the electrons exiting from a transistor to briefly pass through a closed circuit that may be termed a fermionic loop. This loop would differ from the primary superconductive

pathway in that it would be deliberately crippled in terms of its capacity for superconduction. In this and many other types of superconductors, the amount of voltage that may pass through the superconductor as fermions has a particular limit. Electrons exceeding this limit are nevertheless conducted through the material, but they are conducted as standard electrons. This fact may be exploited in order to segregate voltages exceeding pre-set maximums through a shunting mechanism built into one of these closed loops which functions on the basis of foreknowledge of the dilatory timing of the exit of electrons (relative to fermions, which would clear the loop in a lesser length of time.)

The exit apertures of these loops would periodically open and close (by permitting electron flow or blocking it conditionally) according to a timing regime that would permit fermions to proceed but which would block the comparatively slow electrons.

In this way, highly regular quantities of fermionic electrons would be enabled to do their work throughout processor architectures in a fermionic processor by ensuring that the purity of voltage remains constant even after passage through many transistors.

Conclusion

Although fermionic loops are necessary for enabling practical fermionic processors, they may have other applications in areas which require fine control over electron flow, including biomedical studies.